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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,626	07/11/2001	Hideo Taka	35.G2852	7891

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EXAMINER	
NGUYEN, MICHELLE P	
ART UNIT	PAPER NUMBER
2851	

DATE MAILED: 04/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)	
	09/901,626	TAKA, HIDEO	
	Examiner	Art Unit	
	Michelle Nguyen	2851	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

(a) non-volatile memory time-keeping counter circuit

(b) ferroelectric memory time-keeping counter circuit

2. Claim 3 is objected to because in line 6, "clock signal circuit" should be --clock circuit--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "said time-keeping circuit" in line 4. It is not clear to which time-keeping circuit this limitation refers since claim 7 also recites positively the limitations "a time-keeping clock signal generation circuit" and "a ferroelectric memory time-keeping counter circuit" in lines 2 and 3, respectively.

Further, claim 7 recites the limitation "a ferroelectric memory time-keeping counter circuit that forms and stores a time signal" in lines 3-4. It is understood from

applicant's disclosure that only the time-keeping clock signal generation circuit, and not the ferroelectric memory circuit, that forms a time signal (see Pg. 7, lines 11-13).

Claims 8-10 include all limitations set forth in claim 7, thereby rendering the claims indefinite.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,854,950 to Handa et al.

With regard to claim 1, Handa et al. disclose an electronic apparatus comprising:

a clock circuit (quartz crystal oscillator 18, oscillation circuit 19, frequency divider circuit 20) that generates a clock signal having clock signal pulses generated at a predetermined cycle (see Col. 2, lines 4-7, Fig. 2); and

a non-volatile memory time-keeping counter circuit (time counter 161, storage circuit 33) for counting clock signal pulses generated by said clock circuit and storing a count of the clock signal pulses (see Col. 2, lines 4-7, Col. 4, lines 48-51, Fig. 2).

With regard to claim 3, Handa et al. do not teach explicitly a control circuit for controlling the electronic apparatus according to claim 1, wherein the control circuit controls the non-volatile memory time-keeping counter circuit so as to count the clock

signal pulses in response to the clock signal generated by the clock signal circuit. However, it is understood that an electronic device requires a control circuit for enabling operation of the electronic device. Further, it is understood that a circuit having a counter and a memory requires a control circuit for enabling the counting of pulses, and the storage and reading of data. Therefore, a control circuit as claimed is inherent to the structure of the electronic apparatus of Handa et al.

With regard to claim 4, Handa et al. teach the electronic apparatus according to claim 1 to comprise a camera (camera 1A) (see Col. 3, lines 33-5, Figs. 1, 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handa et al. in view as applied to claim 1 above, and further in view of U.S. Patent No. 5,942,877 to Nishimura.

With regard to claim 2, Handa et al. do not teach the non-volatile memory time-keeping circuit as discussed above with respect to claim 1 to comprise a ferroelectric memory. Instead, Handa et al. teach the non-volatile memory time-keeping circuit to comprise an EEPROM (see Col. 4, lines 50-1). However, Nishimura teaches a ferroelectric RAM and an EEPROM to be art-recognized equivalents (see Col. 1, lines 28-33). Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to substitute into the non-volatile memory time-keeping circuit of Handa et al. a ferroelectric memory for the EEPROM as taught by Nishimura for providing an alternative means for reading and storing data.

9. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handa et al. as applied to claims 1 and 4 above, respectively, and further in view of U.S. Patent No. 4,825,233 to Kanai et al.

With regard to claims 3 and 5, Handa et al. do not teach explicitly a control circuit for controlling the electronic apparatus according to claims 1 and 4, respectively. However, Kanai et al. teach an electronic apparatus (camera) to comprise a control circuit comprising a central processing unit (CPU 18) for controlling the electronic apparatus, wherein the control circuit controls a non-volatile memory time-keeping counter circuit so as to count (via pulse counter) the clock signal pulses in response to the clock signal generated (via clock pulse generator 16) by the clock circuit (see Col. 2, lines 59-66, Fig. 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate into the electronic apparatus of Handa et al. a control circuit as taught by Kanai et al. for enabling operation of the electronic apparatus, including the counting of pulses and the storage and reading of data.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handa et al. as applied to claim 1 above, and further in view of Japanese Patent Publication No. 06-250278 to Kitani et al. (computer-generated translation provided).

With regard to claim 6, Handa et al. do not teach a predetermined value to be added to the memory contents of the non-volatile memory time-keeping counter circuit as discussed above with respect to claim 1 when a power supply battery for supplying power to the electronic apparatus is replaced. However, Kitani et al. teach a non-volatile memory time-keeping counter circuit to start counting in a state in which a predetermined value is added to the memory contents of the non-volatile memory time-keeping circuit when a power supply (power cell 43) for supplying power to an electronic apparatus (camera) is replaced for eliminating the need for a backup supply voltage while still maintaining accuracy during time-keeping (see Pg. 8, lines 4-13, Pg. 9, lines 4-6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate into the electronic apparatus of Handa et al. a non-volatile memory time-keeping circuit as taught by Kitani et al. for eliminating the need for a backup power supply.

11. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,854,950 to Handa et al. in view of U.S. Patent No. 5,942,877 to Nishimura.

With regard to claim 7, Handa et al. disclose an electronic apparatus comprising:

a time-keeping clock signal generation circuit (quartz crystal oscillator 18, oscillation circuit 19, frequency divider circuit 20) that keeps time (see Col. 2, lines 4-7, Fig. 2); and

a memory time-keeping counter circuit (storage circuit 33, time counter 161) that forms and stores a time signal concerning time kept by the time-keeping circuit (see Col. 2, lines 4-7, Col. 4, lines 48-51, Fig. 2).

Handa et al. do not teach the memory time-keeping counter circuit to comprise a ferroelectric memory. Instead, Handa et al. teach the memory time-keeping counter circuit to comprise an EEPROM (see Col. 4, lines 50-1). However, Nishimura teaches a ferroelectric RAM and an EEPROM to be art-recognized equivalents (see Col. 1, lines 28-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute into the memory time-keeping counter circuit of Handa et al. a ferroelectric memory for the EEPROM as taught by Nishimura for providing an alternative means for reading and storing data.

With regard to claim 8, Handa et al. do not teach explicitly a control circuit for controlling the electronic apparatus according to claim 7, wherein the control circuit controls the memory time-keeping counter circuit so as to store the time signal for said time-keeping clock signal generation circuit in response to time-keeping by said time-keeping clock signal generation circuit. However, it is understood that an electronic device requires a control circuit for enabling operation of the electronic device. Further, it is understood that a circuit having a counter and a memory requires a control circuit for enabling the counting of pulses, and the storage and reading of data. Therefore, a control circuit as claimed is inherent to the structure of the electronic apparatus of Handa et al.

With regard to claim 9, Handa et al. teach the electronic apparatus according to claim 7 to comprise a camera (camera 1A) (see Col. 3, lines 33-5, Figs. 1, 2).

12. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handa et al. in view of Nishimura as applied to claim 7 above, and further in view of U.S. Patent No. 4,825,233 to Kanai et al.

With regard to claims 8 and 10, Handa et al. do not teach explicitly a control circuit for controlling the electronic apparatus according to claim 1. However, Kanai et al. teach an electronic apparatus (camera) to comprise a control circuit comprising a central processing unit (CPU 18) for controlling the electronic apparatus, wherein the control circuit controls a memory time-keeping counter circuit so as to store (via registers 18A, 18B) a time signal for a time-keeping clock signal generation circuit (clock pulse generator 16) in response to time-keeping by said time-keeping clock signal generation circuit (see Col. 2, lines 59-66, Fig. 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate into the electronic apparatus of Handa et al. a control circuit as taught by Kanai et al. for enabling operation of the electronic apparatus, including the counting of pulses and the storage and reading of data.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Nguyen whose telephone number is 703-305-2771. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Russ Adams can be reached on 703-308-2847. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4900.

mpn
April 7, 2003

RUSSELL ADAMS
SUPERVISORY PATENT EXAMINER
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